## Use of high-speed counter

| 1) C251 C252 C254 (AB phase) maximum response frequency: 120 KHz |  |  |  |
| :---: | :---: | :---: | :---: |
| 2) C 253 C 255 (phase AB ) maximum response frequency: 120 KHz |  |  |  |
| 3) C235 C241 C244 C238 (single-phase) maximum response frequency: 120 KHz |  |  |  |
| 4) Maximum response frequency of other high-speed counters: 10 KHz ; |  |  |  |
| 5) The high speed counter of phase AB can be set with 2 -fold frequency and 4 -fold frequency (the setting is only valid in the current cycle of OUT drive): |  |  |  |
| **When M8196 - ON, C251 C252 C254 count pulse 2 frequency multiplication; |  |  |  |
| ${ }^{* *}$ When M8197-ON, frequency doubling of C253 C255 counting pulse 2; |  |  |  |
| ${ }^{* *}$ When M8198- ON, C251 C252 C254 count pulse 4 times frequency; |  |  |  |
| **When M8199 - ON, C253 C255 count pulse 4 times frequency; |  |  |  |
| M0 |  |  |  |
| (C251 K10000000) |  |  |  |
| Example: If an AB phase encoder is used, it will generate 1024 pulses per revolution. If frequency multiplication is n set, the counter will count 1024 <br> (The original FX3U does not support 2-fold frequency). If 2-fold frequency is set, turn the counter for 2048; If the frequency multiplication is set to 4 , turn it once <br> Counter count 4096; instructions: |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  | Input signal form | Counting direction |
| One way single input |  | UPIDOWN $\uparrow \uparrow \downarrow T$ | Specify increase/ decrease count through ON/OFF of M8235 ~ M8245 ON: decrease count OFF: increase count |
| One way double input | count |  | As shown in the left figure, count up/down. The counting direction can be set through M8246 ~M8250. ON: count down OFF: count up |
| $\begin{gathered} \text { Two way } \\ \text { double } \\ \text { counting input } \end{gathered}$ | 1 $X$ |  | As shown in the figure on the left, according to the change of $A / B$ phase input state, |
|  | 4 $X$ |  | increased/ decreased, and the counting direction can be entered through lines M8251~ M8255. |


|  | Counter No | distinguish | Input terminal assignment |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | X000 | X001 | X002 | X003 | X004 | X005 | X006 | X007 |
| One way single count input | C235 | H/W | U/D |  |  |  |  |  |  |  |
|  | C236 | S/W |  | U/D |  |  |  |  |  |  |
|  | C237 | S/W |  |  | U/D |  |  |  |  |  |
|  | C238 | H/W |  |  |  | U/D |  |  |  |  |
|  | C239 | S/W |  |  |  |  | U/D |  |  |  |
|  | C240 | S/W |  |  |  |  |  | U/D |  |  |
|  | C241 | H/W | U/D | R |  |  |  |  |  |  |
|  | C242 | S/W |  |  | U/D | R |  |  |  |  |
|  | C243 | S/W |  |  |  |  | U/D | R |  |  |
|  | C244 | H/W | U/D | R |  |  |  |  | S |  |
|  | C245 | S/W |  |  | U/D | R |  |  |  | S |
| One way single count input | C246 | S/W | U | D |  |  |  |  |  |  |
|  | C247 | S/W | U | D | R |  |  |  |  |  |
|  | C248 | S/W |  |  |  | U | D | R |  |  |
|  | C249 | S/W | U | D | R |  |  |  | S |  |
|  | C250 | S/W |  |  |  | U | D | R |  | S |
| Two way double counting input | C251 | H/W | A | B |  |  |  |  |  |  |
|  | C252 | H/W | A | B | R |  |  |  |  |  |
|  | C253 | H/W |  |  |  | A | B | R |  |  |
|  | C254 | H/W | A | B | R |  |  |  | S |  |
|  | C255 | H/W |  |  |  | A | B | R |  | S |
| H/W: Hardware counter S/W: Software counter U: Up counter input D:Minus counter input |  |  |  |  |  |  |  |  |  |  |

Only X0-X5 high-speed function is supported, X6 and X7 do not support high-speed function
Instructions for DHSCS, DHSCR and DHSZ instructions:
${ }^{* *}$ The times of simultaneous driving of three high-speed comparison commands: X0 hardware counter twice, X3 hardware counter twice, and soffware counter four times (greater than 6705);
*When comparing hardware high-speed counters, the response frequency will not change. DHSCS and DHSCR perform real-time comparison, but DHSZ hardware interval comparison is not real-time, but about 5us comparison; ${ }^{* *}$ When the hardware high-speed counter is used, the comparison results will be output as long as DHSCS, DHSCR

